ANDREW CHENG

EDUCATION

Cornell University · B.S and M.Eng in Computer Science · Ithaca, NY August 2020 - May 2024

- GPA: 4.1/4.0, Dean's List All Semesters, ACT: 36, M.S Dual Degree
- Relevant Coursework: **Computer Architecture, Operating Systems, Distributed Systems, Compilers Systems Programming, Embedded Systems**, Object Oriented Programming and Data Structures, Analysis of Algorithms, Functional Programming, Machine Learning, Computer Vision

EXPERIENCE

Software Engineering/FPGA Intern · Citadel Securities May 2023 - August 2023

- Made message parsing go faster with Python, C++, and System-Verilog.

Software Development Engineer Intern · Amazon May 2022 - August 2022

- Rendered API errors from Java backend to display on ReactJS application, increasing submission success rate by 3.4% for over 600,000 daily advertisers.
- Created a campaign submission tracking dashboard, improving response times of on-call engineers by 15%.
- Debugged and solved over 25 tickets on the team's ReactJS application, shortening backlog issues by 6 months.

Computer Architecture Research Intern · Computer Systems Laboratory April 2021 - December 2021

- Implemented Secure Hash Algorithm Two on vectorized assembly, optimizing throughput by 10%.
- Minimized data movement by 15% through the use of data level parallelism on the system microprocessor.

Operating Systems Teaching Assistant · Cornell University December 2020 - Present

- Enhanced students' understanding of computer science by leading weekly discussion sections of 40 people.
- Mentored students within office hours and answered over 25% of all questions posted on the class's public forum.

PROJECTS

Optimizing Compiler · (Java, C++, x86 Assembly) January 2023 - May 2023

- Architected a compiler with over 25,000 lines of code for Eta (based off C) involving lexing, parsing, type-checking.
- Led a team of four utilizing Git, AGILE software practices, and robust end-to-end tests leading to 97% code coverage.
- Integrated advanced optimization techniques, including induction variable elimination, partial redundancy elimination, and graph-coloring register allocation, resulting in a runtime speed improvement of 700 %.

Fault Tolerate Sharded Key/Value Store · (Java, Python) January 2023 - May 2023

- Designed a sharded key/value database that partitions keys over replicas, enhancing system throughput by 500%.
- Utilized the Paxos leader election and log replication to maintain data synchronization within each replica group.

Multicore RISC-V Processor · (C, RISC-V, Python, System-Verilog) August 2022 - December 2022

- Designed and implemented a multicore system for running parallel C applications at the register-transfer level by integrating a quad-core fully bypassed pipelined processor alongside an associative cache and ring network.
- Optimized cache throughput by 300% through improving hit latency and removing redundant FSM states.

Physics Oscillator Simulator · (OCaml, CSV) September 2021 - December 2021

- Developed an interactive physics simulation to model 2-D motion of springs with a team of four.
- Calculated trajectories of a system of masses with only a 0.05% margin of error by applying numeric integration, dynamic programming, and functional programming techniques.

SKILLS

Languages	Python, C/C++, System-Verilog, Java, OCaml, JavaScript
Tools & Technologies	React, Github, NumPy, HTML/CSS, Pytorch, Matplotlib